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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/653,925	09/01/2000	Nikhil Vishwanath Kelkar	NSC1P181/P04767	7254

22434 7590 04/22/2002

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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/653,925	Kelkar et al
Examiner	**Art Unit**
Nitin Par kh	2811

-- The MAILING DATE of this communication appears on th cover sh t with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on Feb 4, 2002

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-20 is/are pending in the applica

4a) Of the above, claim(s) 8-14 is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-7 and 15-20 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 2

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Takeda et al (US Pat. 5892271).

Regarding claim 1, Takeda et al disclose an integrated circuit (IC) package comprising:

- an IC die (1 in Fig. 3/4) having a top side and bottom side opposite to the top side, the top side including bond pads/terminal electrodes (2 in Fig. 3/4)
- raised interconnects/projection bumps (3 in Fig. 3/4) located over and conductively coupled to the bond pads
- a flexible circuit film/substrate (4/8 in Fig. 3/4) being located over and conductively attached to the raised interconnects/projection bumps such that an air gap is formed between the IC die and the flexible circuit film/substrate, and

- contact/external connection bumps (7 in Fig. 3/4) conductively coupled to the outer landings/terminal electrodes (Col. 4, line 26)

(Fig. 3/4; Col. 3, line 50- Col. 4, line 50).

3. Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by DiStefano et al (US Pat. 5518964).

Regarding claim 15, DiStefano et al disclose an integrated circuit (IC) wafer (86 in Fig. 11-14) having a top side and bottom side opposite to the top side, the wafer comprising:

- a plurality of IC dice (88 in Fig. 11-14) having a plurality of bond pads/contacts (90 in Fig. 14)

- a plurality of raised interconnects/projection bumps (104 in Fig. 14) located over and conductively coupled to the bond pads, and

- a composite flexible circuit/dielectric film (34/60 in Fig. 14) being applied over and conductively attached to the plurality of raised interconnects/projection bumps such that an air gap is formed between the IC wafer and the flexible circuit film/substrate

(Fig. 14 and 11-13; Col. 11, line 1- Col. 12, line 58).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeda et al (US Pat. 5892271) in view of Akagawa et al (US Pat. 5834844).

Regarding claim 2, Takeda et al further disclose the air gap/height being in a range of 40-50 microns but fail to specify the range being 10-500 microns.

The parameters such as air gap/spacing between the die and the substrate, bump height, bump/pad spacing/pitch/offset, size/dimension of the die/substrate, etc. in chip packaging and interconnection technology art are a matter of design choice to achieve the overall package size, interconnection density and reliability requirements.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to select the air gap/height being in a range of 10-500 microns to achieve the overall package size, interconnection density and reliability in Takeda et al's package.

Regarding claim 3, Takeda et al disclose the size of the flexible circuit film/substrate being slightly larger than that of the die but fail to specify the respective sizes being substantially the same.

However, Takeda et al further disclose using the film/substrate being slightly smaller or same as that of the die (Fig. 5 and 8 respectively).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to select the flexible circuit film being of the same size as the die to achieve the desired mounting area and interconnection density in Takeda et al's package.

Regarding claims 4-6, Takeda et al disclose the flexible circuit film/substrate (4/8 in Fig. 3/4) having a top and bottom surfaces and comprising inner landing/electrode terminals located on the bottom surface (not numerically referenced in Fig. 3/4; Col. 4, line 1-25) but fail to show the details/structure of the top surface and outer landing where the outer landing is offset from the inner landing by a horizontal distance in a range of 50-1000 microns.

However, Takeda et al further disclose the film/substrate (4/8 in Fig. 8) having conventional inner and outer landings (14 and 6 respectively in Fig. 8; Col. 6, line 65) which are horizontally offset; the inner landings being interconnected to outer

landing/electrode terminals located on the top surface, and the contact bumps (13 in Fig. 8) being conductively coupled with the outer landings of the film/substrate.

Furthermore, as explained above for claims 1 and 2, the parameters such as air gap/spacing between the die and the substrate, bump height, bump/pad spacing/pitch/offset, size/dimension of the die/substrate, etc. in chip packaging and interconnection technology art are a matter of design choice to achieve the overall package size, interconnection density and reliability requirements.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to select the outer landing being offset from the inner landing by a horizontal distance in a range of 50-1000 microns to achieve the overall package size, interconnection density and reliability in Takeda et al's package.

Regarding claim 7, Takeda et al disclose the bond pad but fail to specify using an under bump pad formed over the bond pad and being conductively coupled to the bond pad and the raised interconnect.

Akagawa et al teach using a variety of conventional configurations where the under bump pads (60 in Fig. 22) are formed over the bonding pad/landing portions and being conductively coupled to the raised interconnects/projection bumps (Fig. 22 and 26-28; Col. 8, line 26-40).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the under bump pads over the bond pad which are conductively coupled to the bond pad and the raised interconnect to improve the bond strength and reliability using Akagawa et al's pad structure in Takeda et al's package.

6. Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over DiStefano et al (US Pat. 5518964) in view of Akagawa et al (US Pat. 5834844).

Regarding claim 16, DiStefano et al fail to specify the range of the air gap/height being 10-500 microns.

The parameters such as air gap/spacing between the wafer/die and the substrate, interconnect/bump height, bump/pad spacing/pitch/offset, size/dimension of the wafer, die, substrate, etc. in wafer/chip scale packaging technology art are a matter of design choice to achieve the overall package size, interconnection density and reliability requirements.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to select the air gap/height being in a range of 10-500 microns to achieve the overall package size, interconnection density and reliability in DiStefano et al's package.

Regarding claim 17, DiStefano et al disclose the bond pad in the form of under bump pads but fail to specify using an under bump pad formed over the bond pad and conductively coupled to the bond pad and the raised interconnect.

Akagawa et al teach using a variety of conventional configurations where the under bump pads (60 in Fig. 22) are formed over the bonding pad/landing portions and being conductively coupled to the raised interconnects/projection bumps (Fig. 22 and 26-28; Col. 8, line 26-40).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the under bump pads over the bond pad which are conductively coupled to the bond pad and the raised interconnect to improve the bond strength and reliability using Akagawa et al's pad structure in DiStefano et al's package.

Regarding claims 18-20, DiStefano et al disclose the flexible circuit film (34/60 in Fig. 14) having a top and bottom surfaces and comprising a plurality of inner landing/electrode leads located on the bottom surface (60 in Fig. 14; Col. 11, line 56) and outer landings on the top surface (44/56 in Fig. 10 and 14; Col. 9) where the film is attached/coupled to the plurality of the raised interconnects/projection bumps at the plurality of inner landing/electrode leads (Col. 11 and 12).

DiStefano et al further disclose a plurality of conventional solder balls/contact bumps (116 in Fig. 17; Col. 14, line 55) being formed and coupled with the outer landings where the outer landings are horizontally offset from the inner landings located at the raised interconnects/bumps but fail to specify the offset of horizontal distance being in a range of 50-1000 microns.

As explained above for claims 15 and 16, the parameters such as air gap/spacing between the wafer/die and the substrate, interconnect/bump height, bump/pad spacing/pitch/offset, size/dimension of the wafer, die, substrate, etc. in wafer/chip scale packaging technology art are a matter of design choice to achieve the overall package size, interconnection density and reliability requirements.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to select the outer landing being offset from the inner landing by a horizontal distance in a range of 50-1000 microns to achieve the overall package size, interconnection density and reliability in DiStefano et al's package.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

04-16-02

Steven Loke
Primary Examiner